the differences between the disclosed embodiments and the prior art subject matter, do not define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

Problems exist in electrical power consumption in the operation of field emission displays. Applicants solve this problems by reducing the capacitance of emitter conductors in the field emission display by decreasing the dielectric constant of a dielectric used in the display. As shown in Figure 7, in one embodiment Applicants teach forming voids or pores in a silicon layer by etching the layer until a porosity of greater than 50% is achieved. (*see* page 6, lines 5-9). The porous silicon layer can then oxidized by conventional thermal oxidation at a temperature in excess of 950-1000°C. (*see* page 6, lines 10-12). In another embodiment, the porous silicon layer can be oxidized in an inductively-coupled oxygen-argon mixed plasma. (*see* page 6, lines 12-15). In yet another embodiment, oxidation can occur in an electron cyclotron resonance nitrous oxide plasma. (*see* page 6, lines 16-18). Accordingly, a silicon layer having 50% voids will, after complete oxidation, result in the porous silicon dioxide layer having approximately 22.5% voids. (*see* page 6, line 29 through page 7, line 1). The end result of these etching and oxidation steps is the creation of a porous silicon dioxide layer having a relative dielectric constant that is substantially reduced compared to a dielectric layer formed from silicon dioxide incorporating no voids. (*see* page 7, lines 4-7). Further, in an optional step, the porous silicon dioxide layer can be planarized. (*see* page 7, lines 14-15).

Jones '524

Jones (U.S. Patent No. 5,529,524) teaches field emission-based flat panel displays and methods of their manufacture. As best shown in Figure 131, Jones '524 teaches a film layer 354 which can be non-conductive (such as undoped amorphous silicon or a non-conductive photopolymer) or conductive (such as aluminum, sputtered doped silicon, or conductive polymer) disposed between a substrate 350 and emitter tips 355. (*see* column 29, lines 7-8 and column 29, lines 38-44). The film layer 354 is treated with a dopant or reactant which diffuses or otherwise penetrates into regions 362 to increase the conductivity thereof. (*see* column 29, lines 7-12). When the film layer 354 consists of silicon, the portions outside regions 362 may be made less conductive by rendering them porous and oxidizing them in O_3 or H_3O_2. (*see* column

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29, lines 19-24). Jones '524 does not disclose, teach, or fairly suggest the method taught by Applicants. Specifically, Jones '524 does not teach or suggest *etching the silicon layer to form a layer of porous silicon having a porosity of greater than 50%.* Instead, Jones '524 expressly teaches away from the methods taught by Applicants. According to Jones '524 the non-conductive film layer 354 is disposed between the emitter tips 355 and the substrate 350, and thus portions of the non-conductive film layer must be made conductive in order to facilitate the flow of electrical current between the substrate and the emitter tips 355. (*see* column 29, lines 7-12). This is in direct conflict with the purpose of the silicon dioxide layer taught by Applicants which surrounds the emitters but does not contact them, and which is made porous and oxidized in order to increase its insulative qualities and thus decrease its dielectric constant.

Lee

Lee (U.S. Patent No. 5,458,518) teaches a method for producing silicon tip field emitter arrays of micro-triodes by using the oxidized porous silicon layer of a silicon substrate. As best shown in Figures 3-6, Lee teaches forming an approximately 1μm deep porous silicon layer 12 by dipping a P-type silicon substrate 10 in a hydrofluoric acid solution to which electric power is supplied. (*see* column 3, lines 47-56). The porous silicon oxide layer 12 is subsequently oxidized at a temperature of 1,000°C and transformed into a porous silicon oxide layer 24 and a thermal silicon oxide layer 24' of dense microstructure with a thickness of 1,000Å. (*see* column 3, lines 62-66). Subsequently, a thin metal film 22 with a thickness of 3,000Å is deposited on the porous silicon oxide layer 24 and silicon mask patterns 11, and gates are formed by removing metal film 22 from the silicon mask patterns 11 by photo etching. (*see* column 4, lines 8-16). After the mask patterns 11 are removed, portions of the silicon oxide layer 24 and the thermal oxide layer 24' under the removed patterns 11 are also removed by means of etching with a hydrofluoric acid solution forming cathode tips 21. (*see* column 4, lines 17-20). Gates are subsequently formed over the cathode tips 21. (*see* column 4, lines 20-23).

In another embodiment shown in Figures 2A-C, Lee teaches etching the silicon substrate 35 to a depth of 7,000-15,000Å and heating the substrate 35 at a temperature of 900-1050°C to form a thermal oxide layer 37. (*see* column 3, lines 17-22). Subsequently a silicon

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oxide layer 34 is deposited on the thermal oxide layer 37, and thin metal film layers 32 are deposited on the silicon oxide layer 34. (*see* column 3, lines 23-25).

Lee does not disclose, teach, or fairly suggest the apparatus taught by Applicants. Nor does Lee remedy the failed teachings of Jones '524 as discussed above. Specifically, Lee does not teach or suggest *etching the silicon layer to form a layer of porous silicon having a porosity of greater than 50%.* Rather, Lee teaches either: (a) forming an approximately 1μm deep porous silicon layer 12 by dipping a P-type silicon substrate 10 in a hydrofluoric acid solution to which electric power is supplied, and oxidizing the porous layer 12 at a temperature of 1,000°C (*see* column 3, lines 47-56 and column 3, lines 62-66) or (b) depositing a silicon dioxide layer 34 on a thermal oxide layer 37. (*see* column 3, lines 23-25).

Further, one would not be lead to do what Applicants have done by combining Lee and Jones '524, because these two references teach oppositely from one another. For example, according to Lee, both the cathode tips 21 and the silicon dioxide layer 24 are formed in the substrate 10. (*see* column 3, lines 62-66 and column 4, lines 17-20). Conversely, in Jones '524, the emitter tips are formed on the non-conductive film layer 354, which itself is formed on the substrate 350. (*see* column 29, lines 7-8 and column 29, lines 38-44).

Gnade *et al.*

Gnade *et al.* (U.S. Patent No. 5,569,058) teaches the use of low density, high porosity insulating material as the dielectric between a gate and a cathode. As best shown in Figure 3 Gnade *et al.* teaches the use of an aerogel having a low density, a high porosity, and a dielectric constant of less than 2.0 as an insulating layer 48. (*see* column 5, lines 38-47). The aerogel layer 48 along with a precursor is applied over a resistive layer 44, and care is taken so that the aerogel does not dry too quickly. (*see* column 6, lines 28-40). Aging of the aerogel and precursor mixture is preferably accomplished by letting the device with the aerogel deposited thereon sit in a saturated ethanol atmosphere for approximately 24 hours at about 37°C. (*see* column 6, lines 45-48). Other curing techniques can also be used in which the gel is dried under supercritical pressure and temperature conditions, however such drying requires high pressures and is difficult to accomplish in a high production environment. (*see* column 6, lines 58-67).

Gnade *et al.* does not disclose, teach, or fairly suggest the apparatus taught by Applicants. Nor does Gnade *et al.* remedy the failed teachings of Jones '524 and Lee discussed above. Specifically, Gnade *et al.* does not teach or suggest *etching the silicon layer to form a layer of porous silicon having a porosity of greater than 50%.* Rather, Gnade *et al.* teaches aging an aerogel and a precursor mixture by letting the device with the aerogel deposited thereon sit in a saturated ethanol atmosphere for approximately 24 hours at about 37°C. (*see* column 6, lines 45-48).

Moreover, Gnade *et al.* expressly teaches away from Applicants' methods since the aerogel of Gnade *et al.* is not the same as a porous silicon dioxide. More specifically, the aerogel of Gnade *et al.*, is formed by polymerizing a tetraethoxysilane precursor to form a wet gel which is then applied to the substrate assembly and dried thereon. (*see* column 6, line 28 through column 7, line 2). There is no pyrolysis step or other similar oxidation treatment that might conceivably convert the polymerized gel into a porous silicon dioxide but rather the polymerized product would have the structure of cross linked siloxane or silicone. Indeed, an oxidation step to convert the gelled polymer into silicon dioxide would tend to destroy the porous form created by the polymerized gel. Thus, although the aerogel structure may be "silica based" as that term in loosely used by Gnade *et al.*, it is not porous silicon dioxide in a compositional or structural sense. In contrast, the porous silicon dioxide layer of the disclosed invention is a product formed by oxidation of a silicon layer. The structure of the product is properly a SiO_2 layer in a porous form. Therefore, it is not accurate to characterize Gnade *et al.* as describing a porous silicon dioxide layer because one of ordinary skill in the art would not equate the structure or composition of the porous aerogel of Gnade *et al.* with that of the porous silicon dioxide layer of the present invention.

Gnade *et al.* not only fails to disclose porous silicon dioxide, it also teaches away from use of standard silicon dioxide as a gate dielectric in field emission displays because "[a]s the thickness of the gate dielectric for flat panel displays is reduced to accommodate smaller hole diameters, the capacitive coupling present with the use of the standard SiO_2 gate dielectric increases and adversely affects proper device operation." (*see* column 3, lines 33-36).

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Jones *et al.* '608

Jones *et al.* (U.S. Patent No. 5,663,608) teaches field emission electron sources characterized by low-turn-on voltages, low gate-to-source current leakage and low anode-to-gate or source current leakage. As best shown in Figure 23, Jones *et al.* '608 teaches a base layer structure consisting of a smoothing layer 342 of SiO overlaid by a thin SiO_2 layer 344, on the top of which is disposed a conductor line layer 346. (*see* column 15, lines 1-6). On this base layer structure are disposed a layer of SiO_2 348, a layer of SiO 350, a layer of SiO_2 352, a layer of insulator material 354, a gate row conductor 356, an insulating layer 357 and a insulating layer 358. (*see* column 15, lines 6-21). An emitter element 362 formed of Si, SiO or SiO_2 +Cr, SiO+Nb or Au and having a tip portion which may be coated with a low work function material or hole injector material is also formed on the base layer structure. (*see* column 15, lines 27-30).

Jones *et al.* does not disclose, teach, or fairly suggest the apparatus taught by Applicants. Nor does Jones *et al.* remedy the failed teachings of Jones '524, Lee and Gnade *et al* discussed above. Specifically, Jones *et al.* does not teach or suggest *etching the silicon layer to form a layer of porous silicon having a porosity of greater than 50%.* In fact, Jones *et al.* makes no mention of an etching or an oxidation process or of any other steps to increase the porosity of a silicon-based layer.

If the undersigned attorney has overlooked a relevant teaching in the above mentioned references, the Examiner is kindly requested to specifically point out where this teaching may be found.

Turning to the specific claim language, the patentable distinctions between the claimed invention and the applied art will be specifically pointed out

Amended claim 42 recites a method of fabricating a field emission display baseplate comprising forming columns on a substrate, forming a layer of silicon on the columns and the substrate, *etching the silicon layer to form a layer of porous silicon having a porosity of greater than 50%*, oxidizing the porous silicon layer to form a layer of porous silicon dioxide, forming an extraction grid on the porous silicon dioxide layer, etching openings through the porous silicon dioxide and the extraction grid, and forming emitters in the openings in the porous silicon dioxide and the extraction grid. Neither Jones '524, Lee, Gnade *et al.* or Jones *et al.* teaches or suggests etching the silicon layer to form a layer of porous silicon having a porosity of

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greater than 50%. The combination of elements recited in claim 42 is thus neither disclosed nor suggested by Jones '524, Lee, Gnade *et al.* or Jones *et al.*.

Amended claim 52 recites a method of fabricating a porous dielectric layer in a field emission display comprising forming a polycrystalline silicon layer on a substrate and a plurality of columns on the substrate, *forming pores in the polycrystalline silicon layer to form a layer of porous silicon having a porosity of greater than 50%*, and oxidizing the polycrystalline silicon layer to provide a porous silicon dioxide layer. Neither Jones '524, Lee, Gnade *et al.* or Jones *et al.* teaches or suggests forming pores in the polycrystalline silicon layer to form a layer of porous silicon having a porosity of greater than 50%. The combination of elements recited in claim 52 is thus neither disclosed nor suggested by Jones '524, Lee, Gnade *et al.* or Jones *et al.*.

Amended claim 56 recites a method of fabricating a field emission display baseplate comprising forming conductors on a substrate, *forming a porous silicon dioxide layer to form a layer of porous silicon dioxide having a porosity of greater than 22.5% on the conductors and on the substrate*, the porous silicon dioxide layer comprising columnar spacers of silicon dioxide with pores between the columnar spacers, forming an extraction grid on the porous silicon dioxide layer, etching openings through the silicon dioxide and the extraction grid; and forming emitters in the openings in the porous silicon dioxide and the extraction grid. Neither Jones '524, Lee, Gnade *et al.* or Jones *et al.* teaches or suggests forming a porous silicon dioxide layer to form a layer of porous silicon dioxide having a porosity of greater than 22.5% on the conductors and on the substrate. The combination of elements recited in claim 56 is thus neither disclosed nor suggested by Jones '524, Lee, Gnade *et al.* or Jones *et al.*.

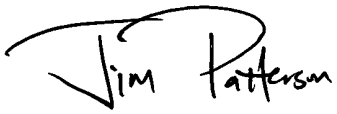
The claims dependant on the independent claims discussed above are also patentable at least because of their dependency on the patentable independent claims, and also on additional grounds because of the additional limitations added by these dependent claims. In the interest of brevity, Applicants do not discuss such other grounds of patentability at the present time, but reserve the right to do so at a later time if necessary.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with Markings to Show Changes Made**".

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

DORSEY & WHITNEY LLP



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

42. (Amended) A method of fabricating a field emission display baseplate comprising:

forming columns on a substrate;

forming a layer of silicon on the columns and the substrate;

etching the silicon layer to form a layer of porous silicon having a porosity of greater than 50%;

oxidizing the porous silicon layer to form a layer of porous silicon dioxide;

forming an extraction grid on the porous silicon dioxide layer;

etching openings through the porous silicon dioxide and the extraction grid; and

forming emitters in the openings in the porous silicon dioxide and the extraction grid.

45. (Amended) The method of claim 42 [wherein the act of oxidizing the porous silicon layer to form a layer of porous silicon dioxide comprises oxidizing a porous polycrystalline silicon layer to form a layer of porous silicon dioxide having an interior volume that is at least 50% voids]further comprising planarizing the silicon dioxide layer.

52. (Amended) A method of fabricating a porous dielectric layer in a field emission display comprising:

forming a polycrystalline silicon layer on a substrate and a plurality of columns on the substrate;

forming pores in the polycrystalline silicon layer to form a layer of porous silicon having a porosity of greater than 50%; and

oxidizing the polycrystalline silicon layer to provide a porous silicon dioxide layer.

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56. (Twice Amended) A method of fabricating a field emission display baseplate comprising:

forming conductors on a substrate;

forming a porous silicon dioxide layer to form a layer of porous silicon dioxide having a porosity of greater than 22.5% on the conductors and on the substrate, the porous silicon dioxide layer comprising columnar spacers of silicon dioxide with pores between the columnar spacers;

forming an extraction grid on the porous silicon dioxide layer;

etching openings through the silicon dioxide and the extraction grid; and

forming emitters in the openings in the porous silicon dioxide and the extraction grid.

62. (Amended) The method of claim 42 wherein [the act of etching the silicon layer forms a porous silicon layer having at least 50% voids and]the act of oxidizing the porous silicon layer forms a porous silicon dioxide layer having at least 22.5% voids.

66. (Amended) The method of claim 46 wherein [the act of etching the polycrystalline silicon layer forms a porous polycrystalline silicon layer having at least 50% voids and]the act of oxidizing the porous polycrystalline silicon layer forms a porous silicon dioxide layer having at least 22.5% voids.

71. (Amended) The method of claim 53 wherein [the act of anodizing the polycrystalline silicon layer forms a porous polycrystalline silicon layer having at least 50% voids and]the act of oxidizing the porous polycrystalline silicon layer forms a porous silicon dioxide layer having at least 22.5% voids.

79. (Amended) The method of claim 56 [wherein the porous silicon dioxide layer comprises at least 22.5% voids]further comprising planarizing the silicon dioxide layer.

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